

CDC 6600

The CDC 6000 series of computers was considered to be the first "supercomputer"

The architecture is designed throughout to operate in parallel

Instructions

Memory references

IO

Arithmetic

Memory words were 60 bits long - longer than most machines of its time period

Addresses were 18 bits long capable of addressing 262144 words of memory

Instructions were 15 or 30 bits long

Registers

Programmer registers

8 60-bit X registers holding either floating or fixed (one's complement) words

8 A registers and 8 B registers each holding 18 bits values

Register B0 was hardwired to 0

An 8 word instruction stack to speed up small loops

When A registers 1-5 were loaded with an address, the corresponding X register was loaded from that address

When A registers 6-7 were loaded with an address, the corresponding X register was stored at that address

There were 15 and 30 bit instructions packed in the 60 bit memory words

15 bit arithmetic instructions referred to three registers

Some 15 bit instructions caused loads or stores at addresses specified by A registers

The 30 bit instructions included an 18 bit displacement convenient for manipulating addresses

Instruction Operation

An instruction is issued to a functional unit when

The specified functional unit is not reserved.

The specified result register is not reserved for a previous result.

Instructions are issued to functional units at minor cycle intervals when no reservation conflicts (above) are present.

Instruction execution starts in a functional unit when both operands are available

execution is delayed when an operand (s) is a result of a previous step which is not complete.

No delay occurs between the end of a first unit and the start of a second unit which is waiting for the results of the first.

No instructions are issued after a branch instruction until the branch instruction has been executed

The branch unit uses

An increment to form the go to K+Bi and go to K if Bi ... instructions, or

The long add unit to perform the go to K if Xi ... instructions in the execution of a branch instruction. The time spent in the long add or increment units is part of the total branch time.

Central memory access read time is computed from end of increment unit time to the time operand is available in X operand register

Minimum time is 500 ns assuming no central memory bank conflict.

Functional units

Two incrementers

Two adders

The floating add unit was 400 ns, yielding an unnormalized sum which could be normalized by a subsequent instruction

Livermore found that most floating adds needed to be normalized.

There were two multiply functional units with 1000 ns latency

There was one divide unit

One shift unit

1 Boolean unit

1 branch unit

Central memory

Central memory was 32 boxes each of 4K 60 bits words for a total of 217 words. The cycle time was 1 microsecond and the memory bus cycle time was 100 ns like the clock of the rest of the machine.

All memories could be operating simultaneously

6600 PPUs

The Peripheral Processing Units were novel in that the ten of them shared execution hardware

Each processor had virtually an 18 bit accumulator, a 12 bit instruction address, and a three bit instruction phase register that was not really visible to the programmer

Each processor had its dedicated box of 4K 12 bit words

There were 12 "channels" which were merely registers that could either drive or be driven by external cables

One PPU instruction was able to either send or receive a block of 12 bits words over one of these channels at one word per microsecond

There was also shared hardware allowing a PPU to move data between central memory and the PPU's private memory

Operating systems dynamically allocated these PPUs to the tasks at hand

IO devices were permanently attached to some cable which in turn was permanently attached to one of these channels.

Physical Characteristics of the CDC 6600

The system was designed around packages of discrete components and transistors.

They were regarded as becoming "reliable"

As the CDC 6600 required 400,000 transistors, it was estimated that the MTBF of the system (based upon transistor reliability) would be over 2000 hours

The logic was Direct Coupled Transistor Logic (DCLT).

There was no byte addressability

If you wanted to store multiple characters in a 60-bit word, you had to shift and mask.

Typically, a six-bit character set was used, which meant no lower-case letters

These systems were meant to be (super)computing engines, not text processors

Functional Units

The 6600/CYBER 74 functional units were: Branch unit (instruction groups 00-07), Boolean unit (10-17), Shift unit

(20-27, 43), FP addition (30-35), Long addition (36-37), FP multiply (40-42), FP divide (44, 45,47), Increment (50-77).

The model 76 types organized this a little different:

Boolean unit (10-17, 25, 27), Shift unit (20-27, 43), Normalize (24,

25),FP add (30-35), Long add (36-37), FP multiply (40-42), FP divide (44, 45), Population count (47), Increment (50-77).